


Revision : 1.11

PAGE	TITLE
------	-------

[illegible]

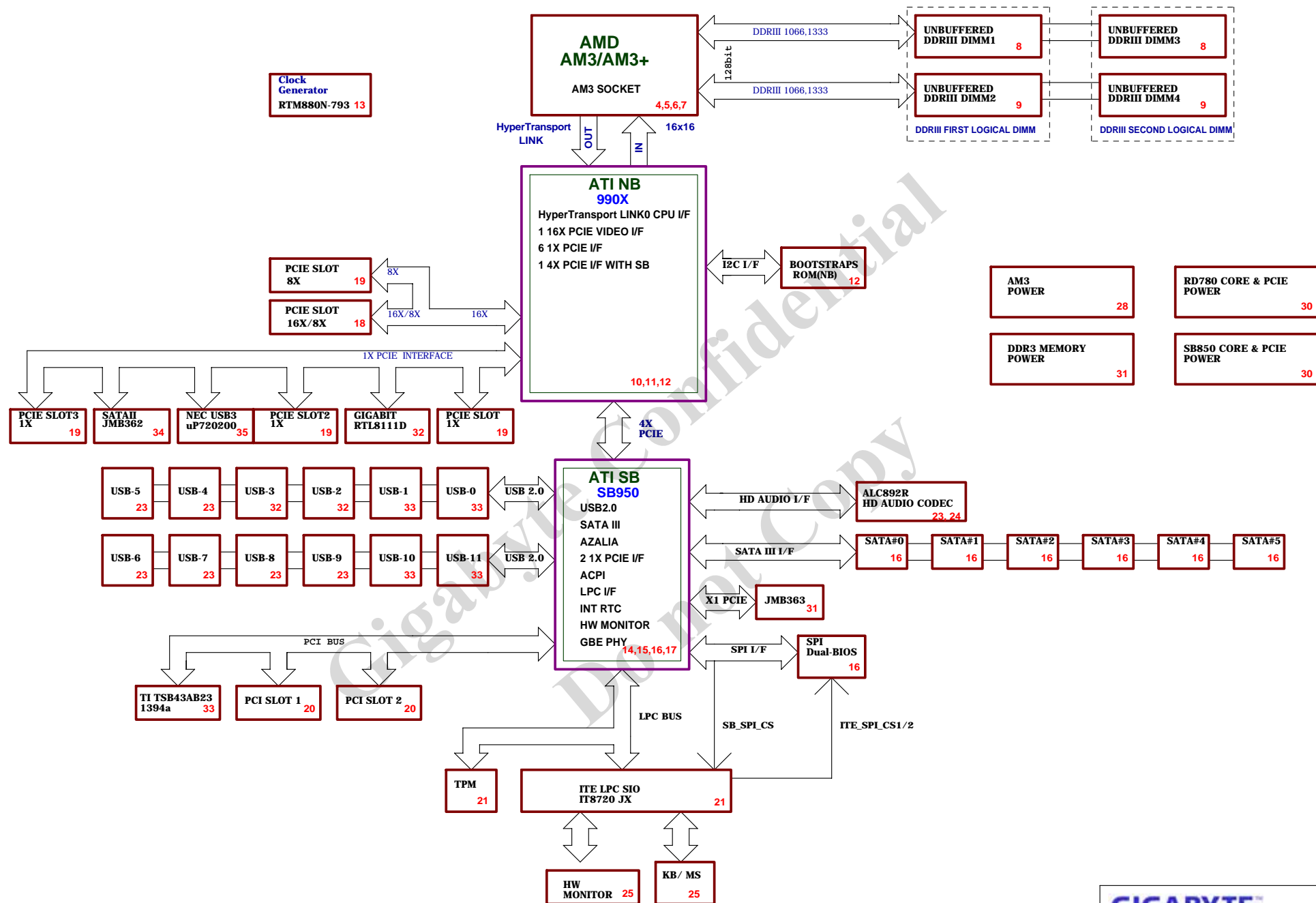
				
Title				
COVER SHEET				
Size	Document Number			Rev
Custom	GA-990XA-UD3			1.11
Date:	Thursday, September 22, 2011	Sheet	1 of 35	

4 Layer, 4mil 50ohm +/- 15% L P-Code: U98094-0

Circuit or PCB layout change for next version

GIGABYTE™

Title			
BOM & PCB HISTORY			
Size	Document Number	Rev	
Custom	GA-990XA-UD3	1.11	
Date:	Thursday, September 22, 2011	Sheet	2 of 35



GIGABYTE™

BLOCK DIAGRAM			
Title	BLOCK DIAGRAM		
Size	Document Number	Rev	
Custom	GA-990XA-UD3	1.11	
Date:	Wednesday, July 20, 2011	Sheet	3 of 35

L0_CADIN_L[0..15] <L0_CADIN_L[0..15] <10>
 L0_CADIN_H[0..15] <L0_CADIN_H[0..15] <10>
 L0_CADOUT_L[0..15] <L0_CADOUT_L[0..15] <10>
 L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] <10>

M2CPUA

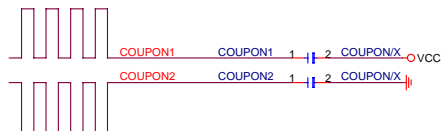
HYPERTRANSPORT

<10> L0_CLKIN_H1	L0_CLKIN_H1 N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5 L0_CLKOUT_H1	>L0_CLKOUT_H1 <10>
<10> L0_CLKIN_L1	L0_CLKIN_L1 P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4 L0_CLKOUT_L1	>L0_CLKOUT_L1 <10>
<10> L0_CLKIN_H0	L0_CLKIN_H0 N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1 L0_CLKOUT_H0	>L0_CLKOUT_H0 <10>
<10> L0_CLKIN_L0	L0_CLKIN_L0 N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1 L0_CLKOUT_L0	>L0_CLKOUT_L0 <10>
<10> L0_CTLIN_H1	L0_CTLIN_H1 V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6 L0_CTLOUT_H1	>L0_CTLOUT_H1 <10>
<10> L0_CTLIN_L1	L0_CTLIN_L1 V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6 L0_CTLOUT_L1	>L0_CTLOUT_L1 <10>
<10> L0_CTLIN_H0	L0_CTLIN_H0 U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2 L0_CTLOUT_H0	>L0_CTLOUT_H0 <10>
<10> L0_CTLIN_L0	L0_CTLIN_L0 V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3 L0_CTLOUT_L0	>L0_CTLOUT_L0 <10>
L0_CADIN_H15 U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5 L0_CADOUT_H15		
L0_CADIN_L15 V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4 L0_CADOUT_L15		
L0_CADIN_H14 T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6 L0_CADOUT_H14		
L0_CADIN_L14 T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6 L0_CADOUT_L14		
L0_CADIN_H13 R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5 L0_CADOUT_H13		
L0_CADIN_L13 T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4 L0_CADOUT_L13		
L0_CADIN_H12 P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6 L0_CADOUT_H12		
L0_CADIN_L12 P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6 L0_CADOUT_L12		
L0_CADIN_H11 M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AE6 L0_CADOUT_H11		
L0_CADIN_L11 M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6 L0_CADOUT_L11		
L0_CADIN_H10 I6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF5 L0_CADOUT_H10		
L0_CADIN_L10 M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4 L0_CADOUT_L10		
L0_CADIN_H9 K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6 L0_CADOUT_H9		
L0_CADIN_L9 K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6 L0_CADOUT_L9		
L0_CADIN_H8 J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5 L0_CADOUT_H8		
L0_CADIN_L8 K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4 L0_CADOUT_L8		
L0_CADIN_H7 U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1 L0_CADOUT_H7		
L0_CADIN_L7 U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1 L0_CADOUT_L7		
L0_CADIN_H6 R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2 L0_CADOUT_H6		
L0_CADIN_L6 T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3 L0_CADOUT_L6		
L0_CADIN_H5 R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1 L0_CADOUT_H5		
L0_CADIN_L5 R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1 L0_CADOUT_L5		
L0_CADIN_H4 N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2 L0_CADOUT_H4		
L0_CADIN_L4 P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3 L0_CADOUT_L4		
L0_CADIN_H3 I1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2 L0_CADOUT_H3		
L0_CADIN_L3 M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3 L0_CADOUT_L3		
L0_CADIN_H2 I3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AE1 L0_CADOUT_H2		
L0_CADIN_L2 L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1 L0_CADOUT_L2		
L0_CADIN_H1 J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2 L0_CADOUT_H1		
L0_CADIN_L1 K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3 L0_CADOUT_L1		
L0_CADIN_H0 J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1 L0_CADOUT_H0		
L0_CADIN_L0 J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1 L0_CADOUT_L0		

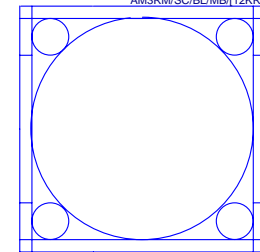
CPU-SK/941AM3/S/GF/[10SC1-A01942-01R_10SC1-A01942-02R]

CPU_VDD_RUN = VCORE
 CPU_VDDA_RUN = VDDA25
 VLDT_RUN = VCC12_HT
 CPU_VDDIO_SUS = DDR15V
 CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
 VLDT_B = HT12B

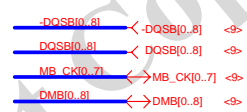
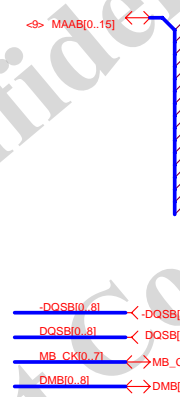


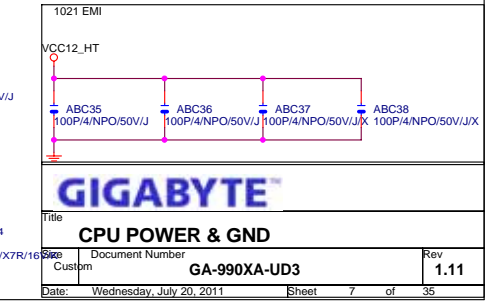
M2CPU
 AM3RM/SC/BL/MB[12KRC-04K812-31R]



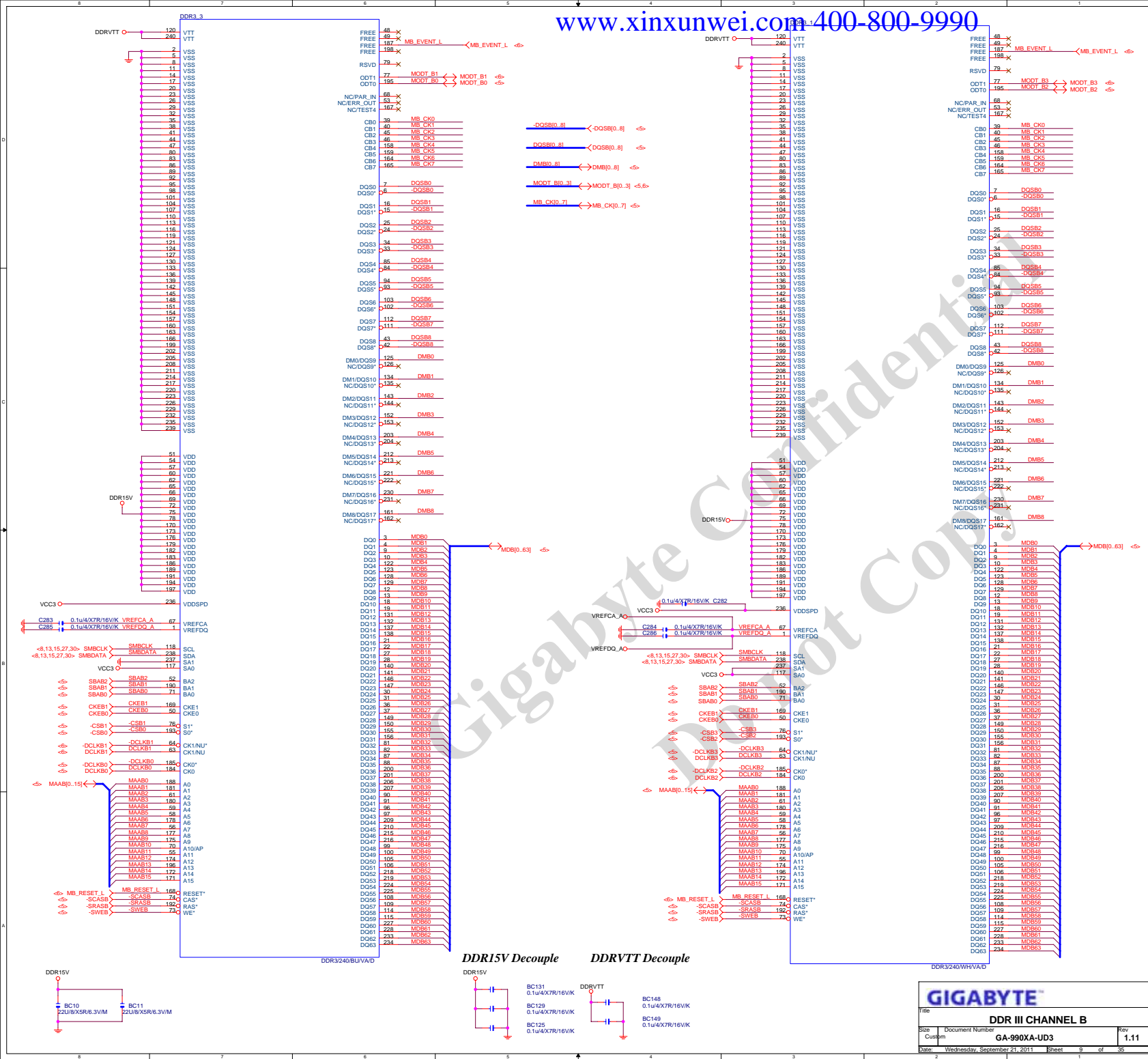
GIGABYTE

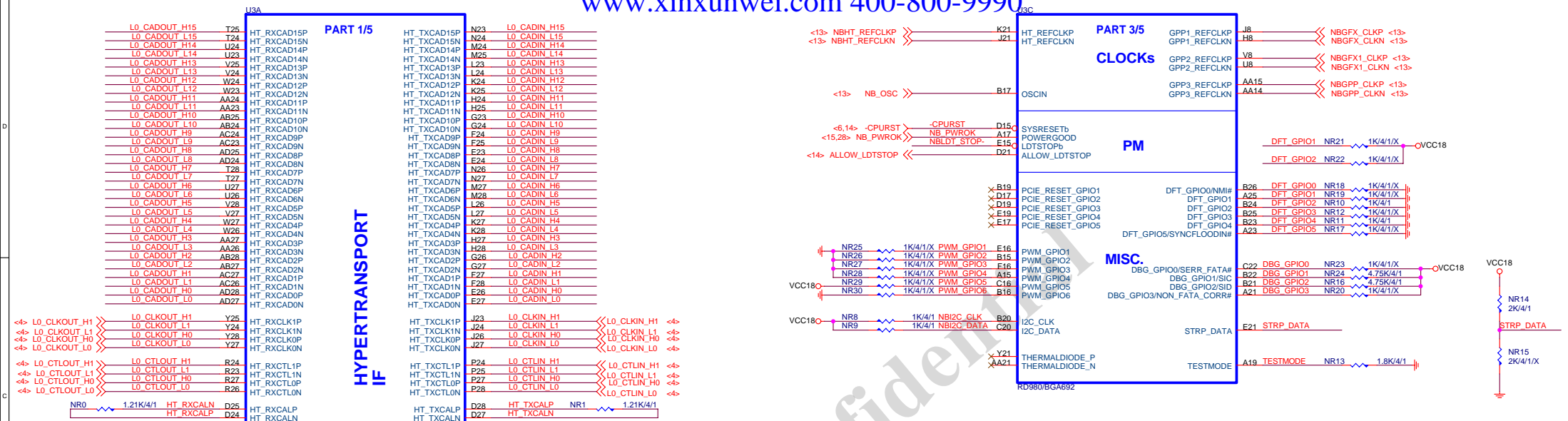
Title			
CPU HYPER TRANSPORT			
Size	Document Number	Rev	
Custom	GA-990XA-UD3	1.11	
Date:	Wednesday, September 21, 2011	Sheet	4 of 35











DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

```

These pin straps are used to configure PCI-E GPP mode.
GPIO4:3:2
000: 4:2:4 B
001: 4:1:1:4 C
010: 1:1:1:1:1:4 L (Hardware Default)
011: 2:1:1:1:1:4 E
100: 2:2:1:1:4 K
101: 2:2:2:4 C2
110: Hardware default (mode L) or EEPROM
111: Hardware default (mode L) or EEPROM
101: 01000
111: 01011

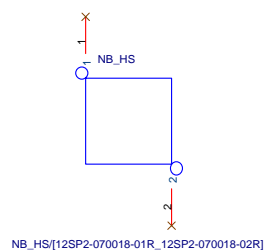
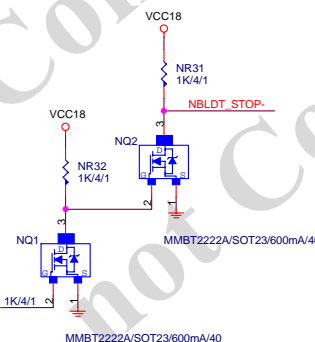
```

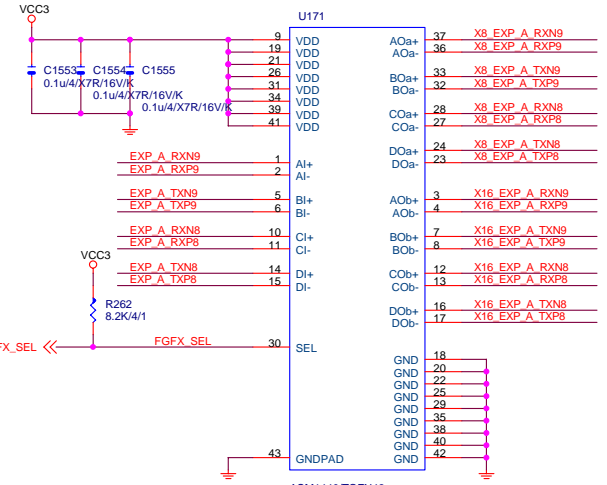
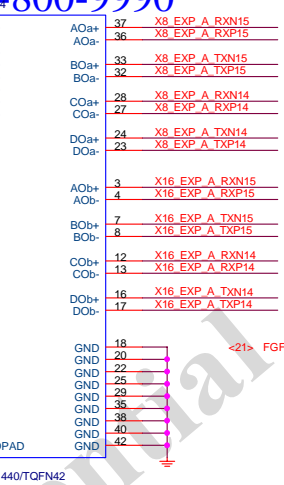
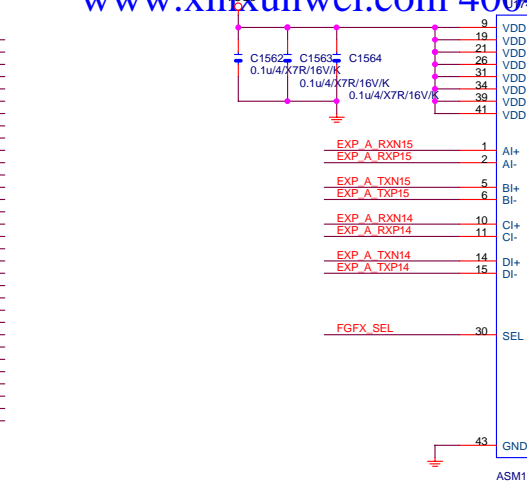
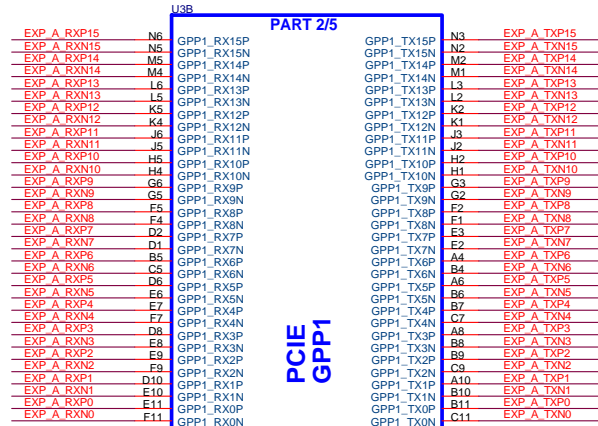
DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

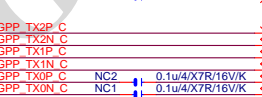
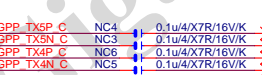
DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

Enables the Test Debug Bus using PCIe bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable





PCI E slot TX need CAP close to slot side



PLACE THESE CAP CLOSE TO NB.

Function	SEL
xI--> xOa	L (X 8)
xI--> xOb	H (X 16)

GIGABYTE

RD990 PCIE I/F ,Switch

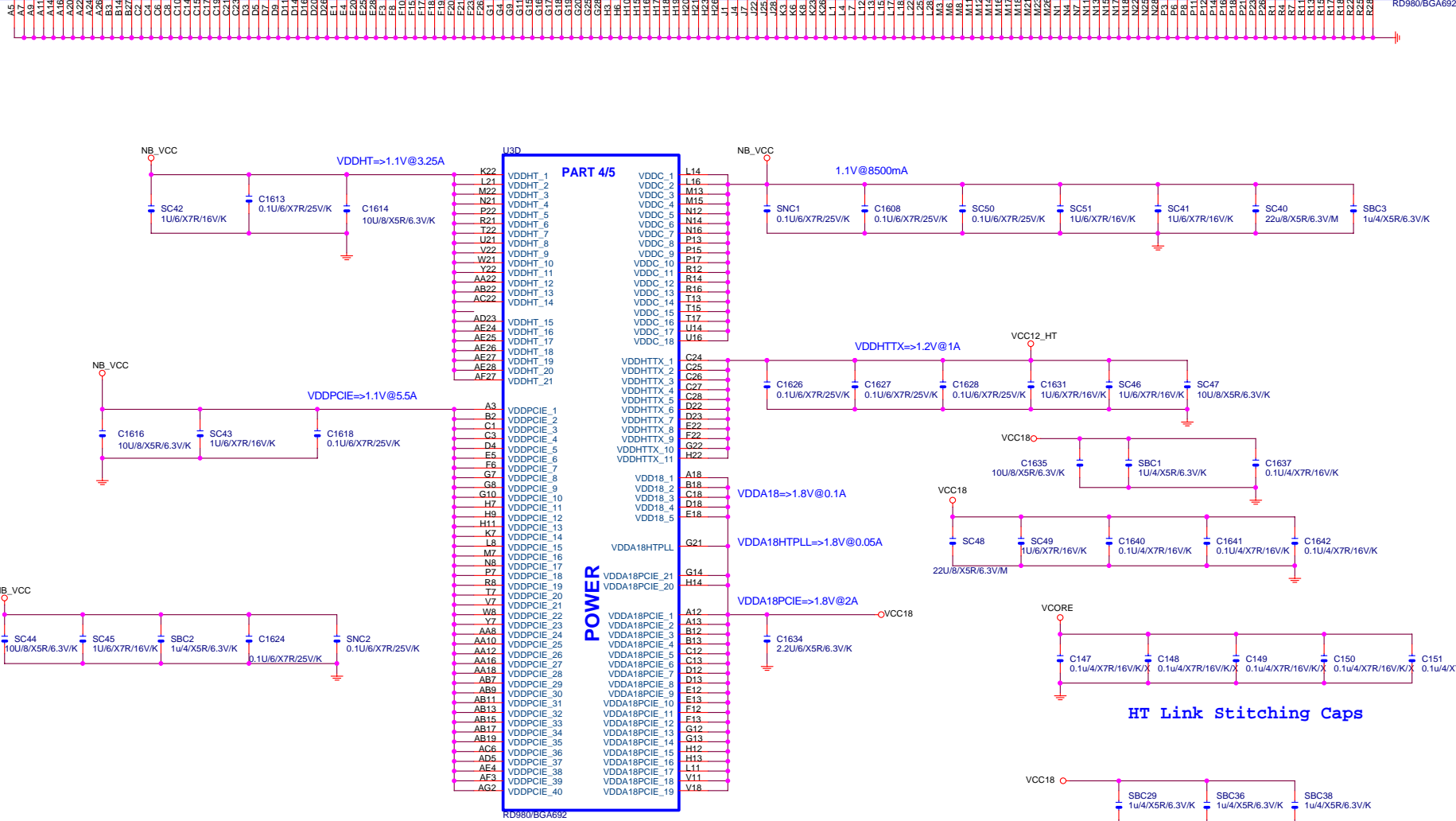
Document Number GA-990XA-UD3

Date: Thursday, September 22, 2011 Sheet 11 of 35

Rev 1.11

PART 5/5

GROUND



GIGABYTE®

Title			RD990 POWER & GND
Size	Document Number	Rev	1.11
Custom	GA-990XA-UD3		
Date:	Thursday, September 22, 2011	Sheet	12 of 35

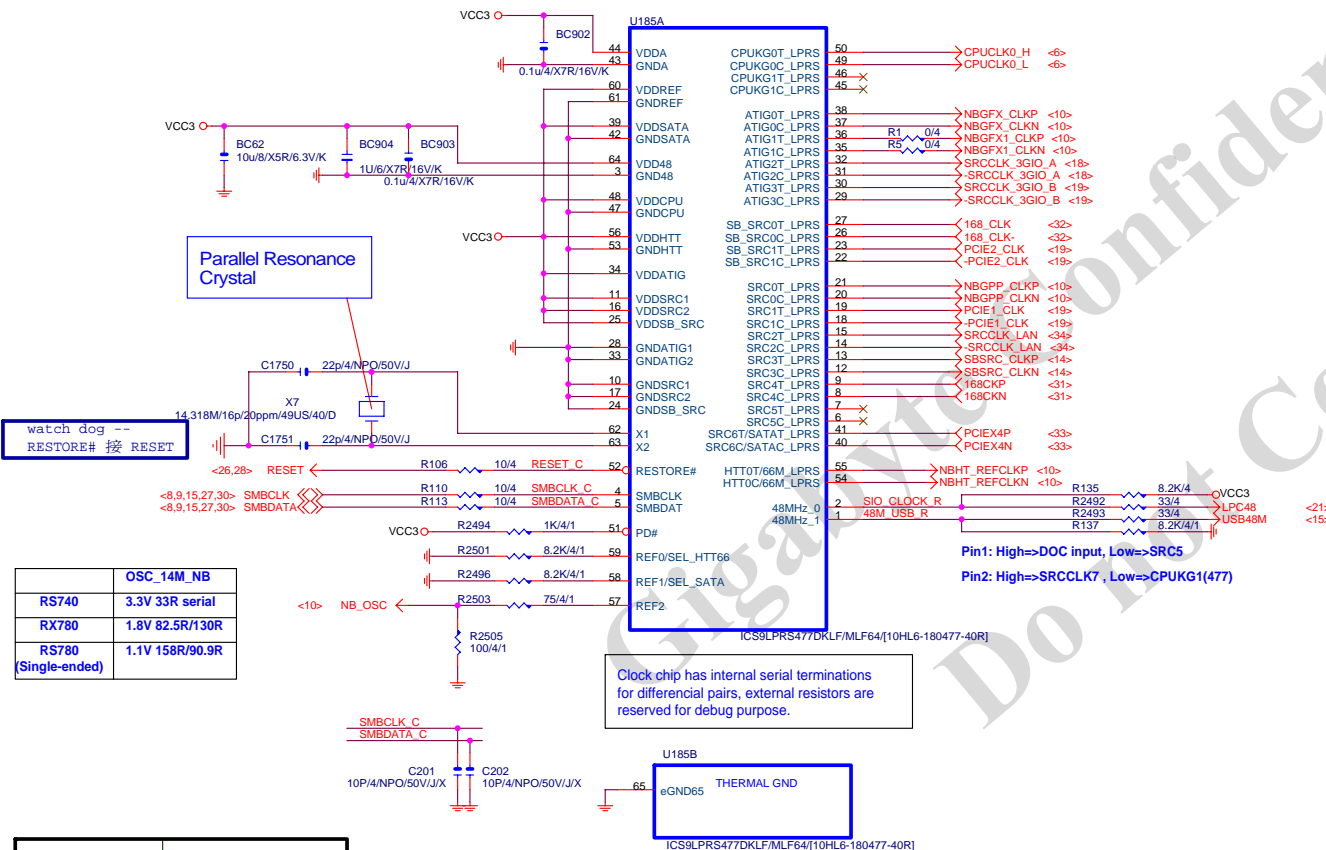
NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases

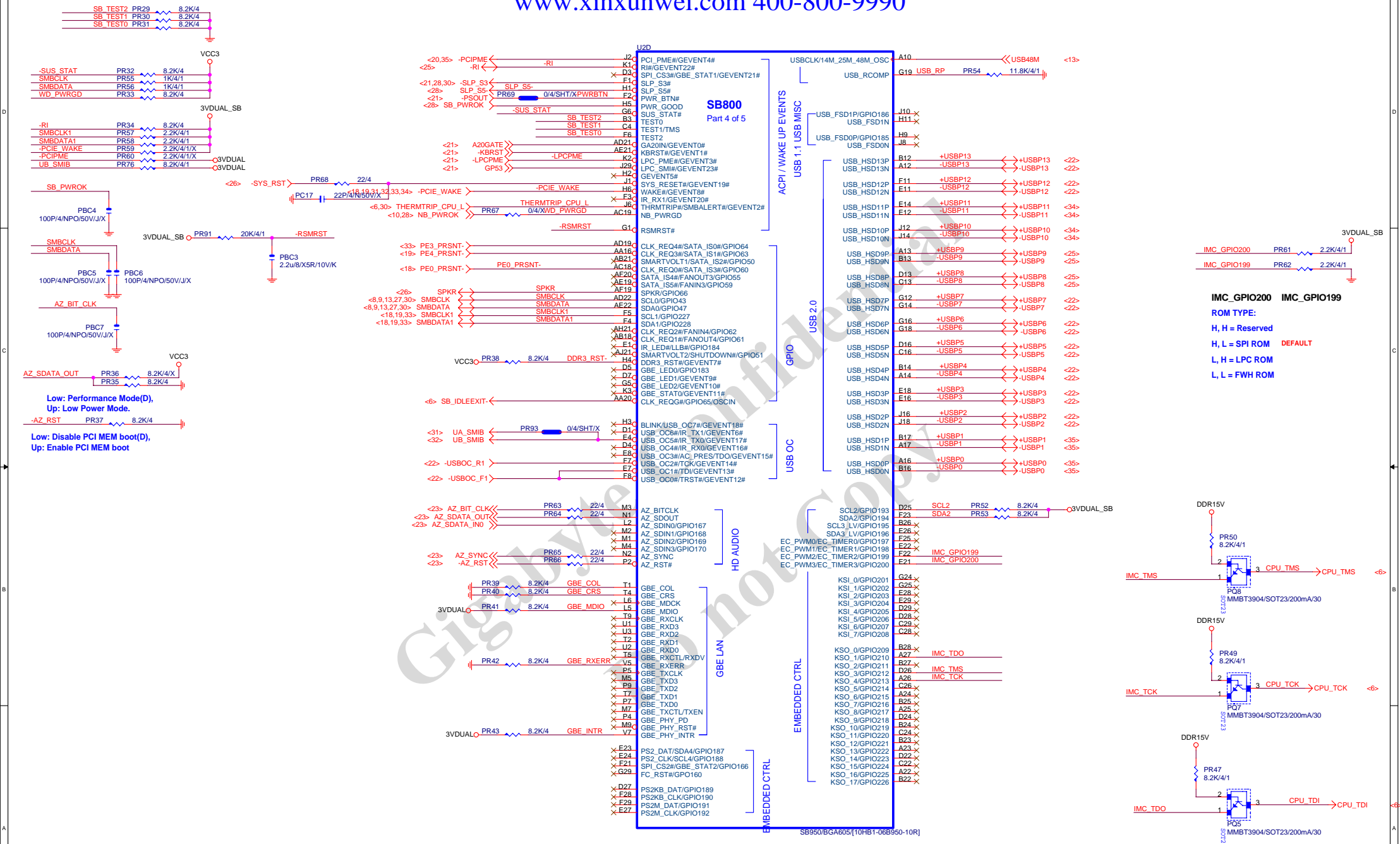
- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

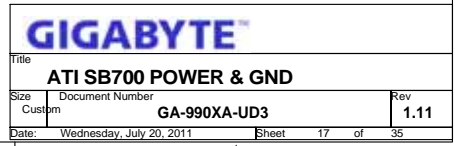
Place R800/801 less than 500 mils away from U800
 R851 less than 100 mils away from R800/801
 route CPU clock as 100ohm differential pair

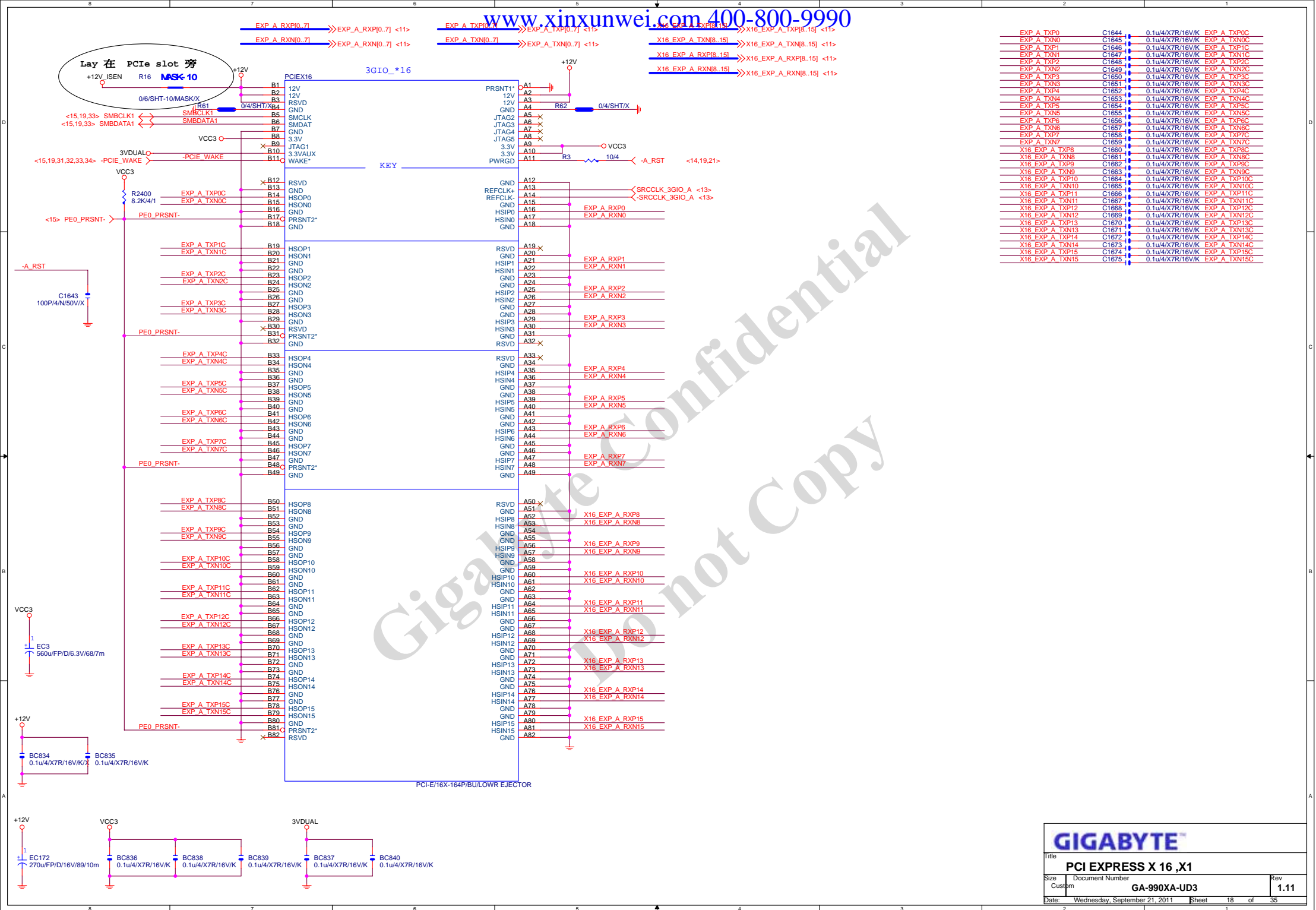


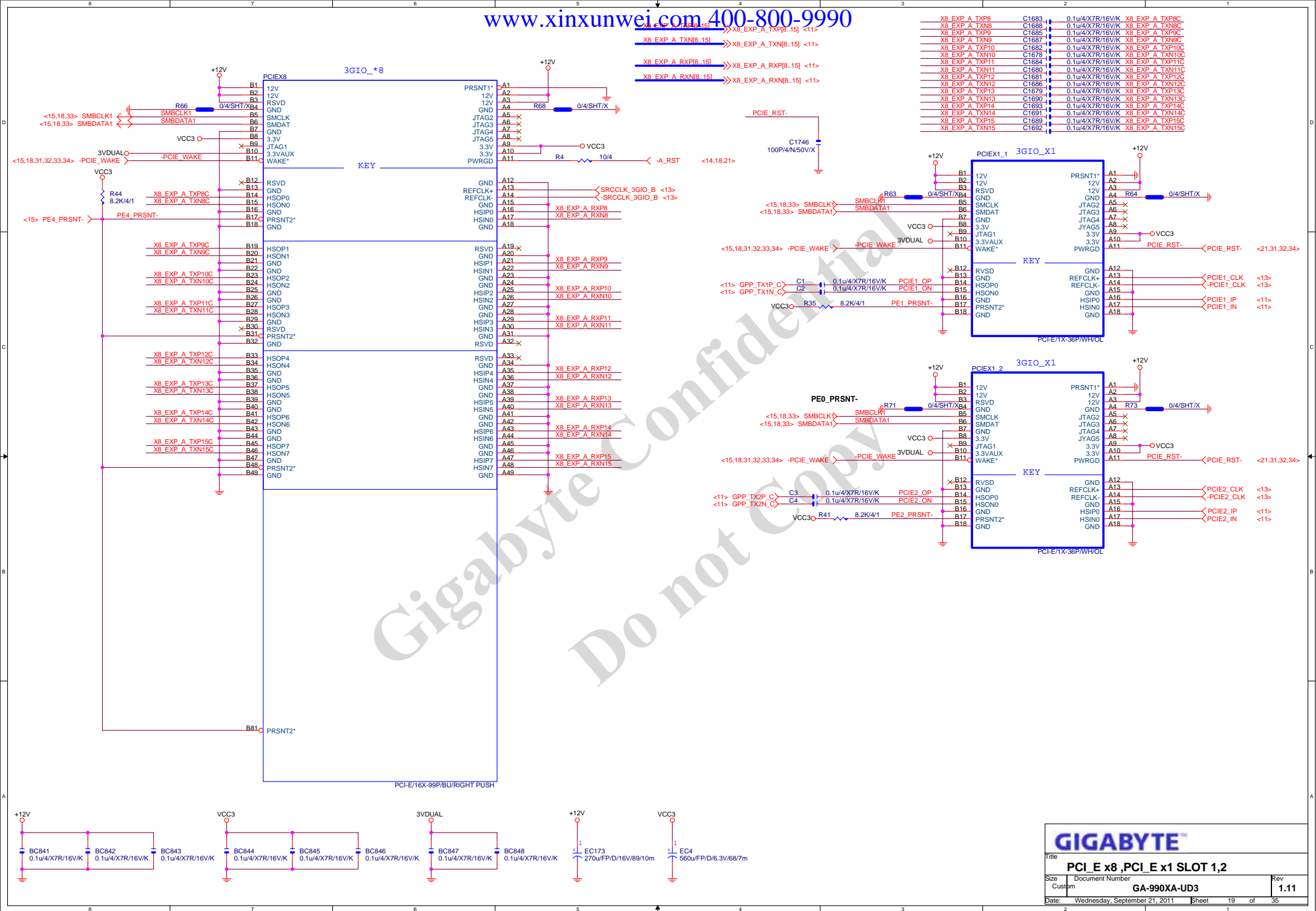
GIGABYTE™

Title			RTM880N-793		
Size	Document Number	GA-990XA-UD3			Rev
Custom					1.11
Date:	Wednesday, September 21, 2011	Sheet	13	of	35





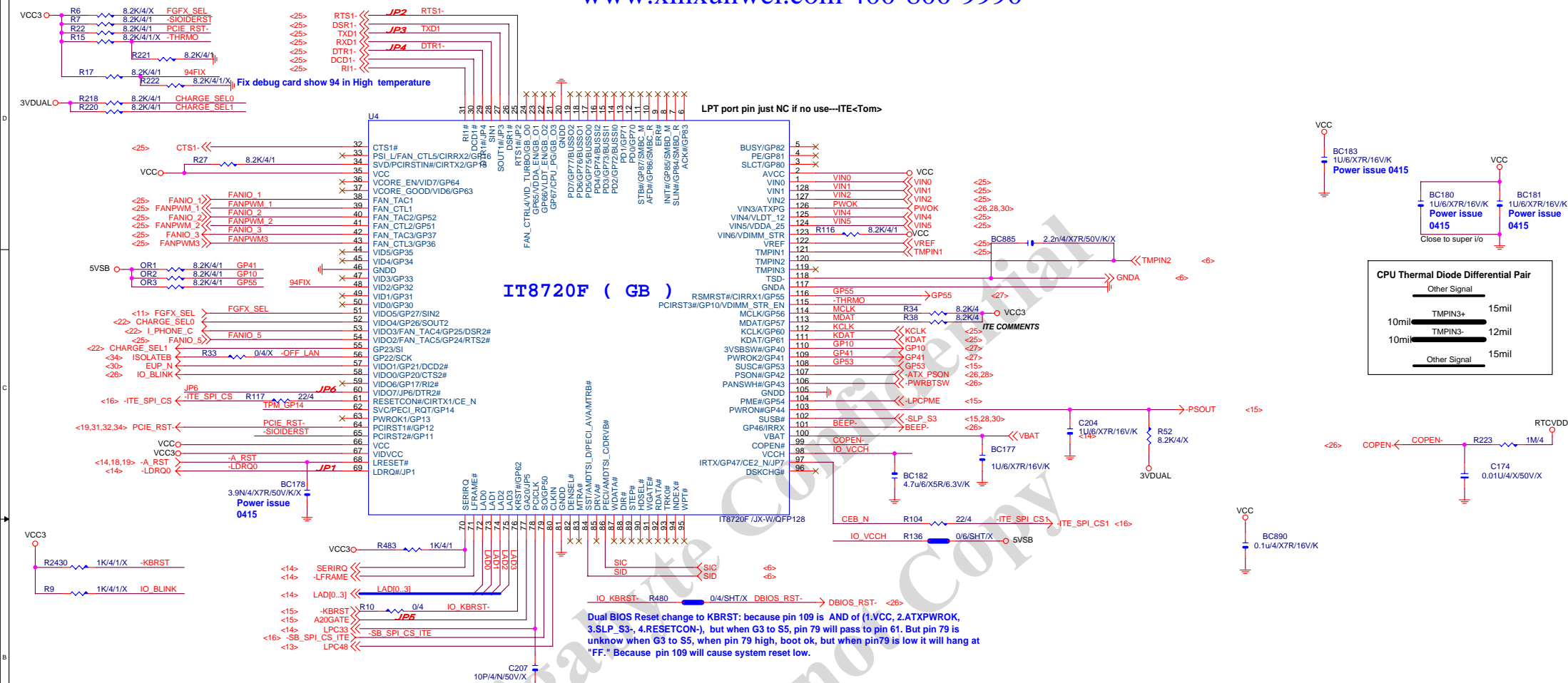




GIGABYTE

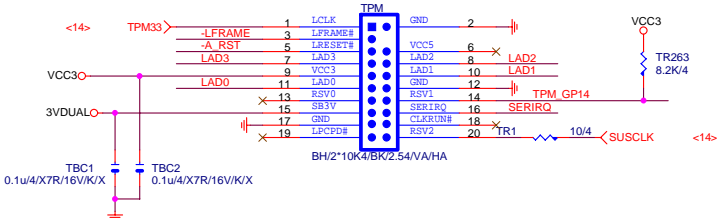
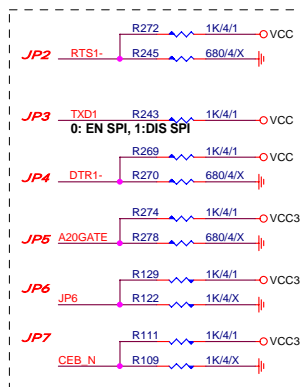
PCI_E x8 ,PCI_E x1 SLOT 1,2

Title	Document Number	Rev
Custom	GA-990XA-UD3	1.11
Date:	Wednesday, September 21, 2011	Sheet 19 of 35



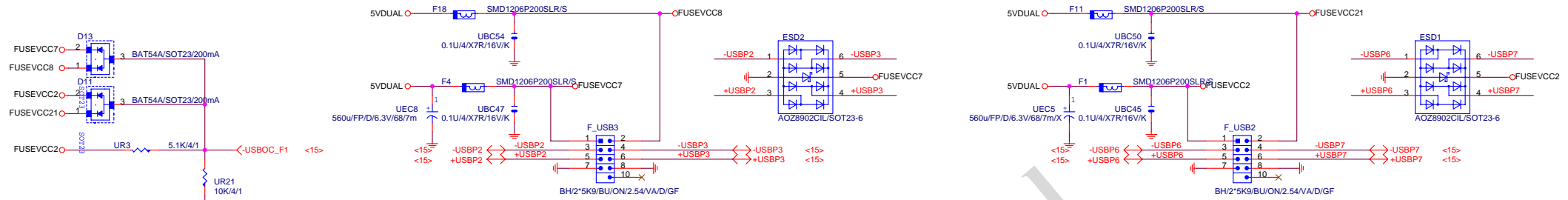
IT8720GB Power On Strapping Options

Symbol	value	Description
JP1		
Pin 69		
JP2	1	Disable VID output pins
Pin 25	0	Enable VID output pins
JP3	1	Disabled.
Pin 27	0	Flash I/F Address Segment 1 is enabled
JP4	1	K8 power sequence disabled
Pin 29	0	K8 power sequence enabled
JP3 & JP5	11 Half Run	Default value of EC Index 15h/16h/17h is 40h
Pin 27 & Pin 77	10 No Run	Default value of EC Index 15h/16h/17h is 7Fh
	01 Full Run	Default value of EC Index 15h/16h/17h is 00h
	00 75% Run	Default value of EC Index 15h/16h/17h is 20h
JP5	1	Disable WDT to rest PWROK
Pin 77	0	Enable WDT to rest PWROK
JP6	1	Disable SVID Function
Pin 60	0	Enable SVID Function
JP7	1	Enable Dual BIOS Function for GigaByte Only
Pin 97	0	Disable Dual BIOS Function for GigaByte Only

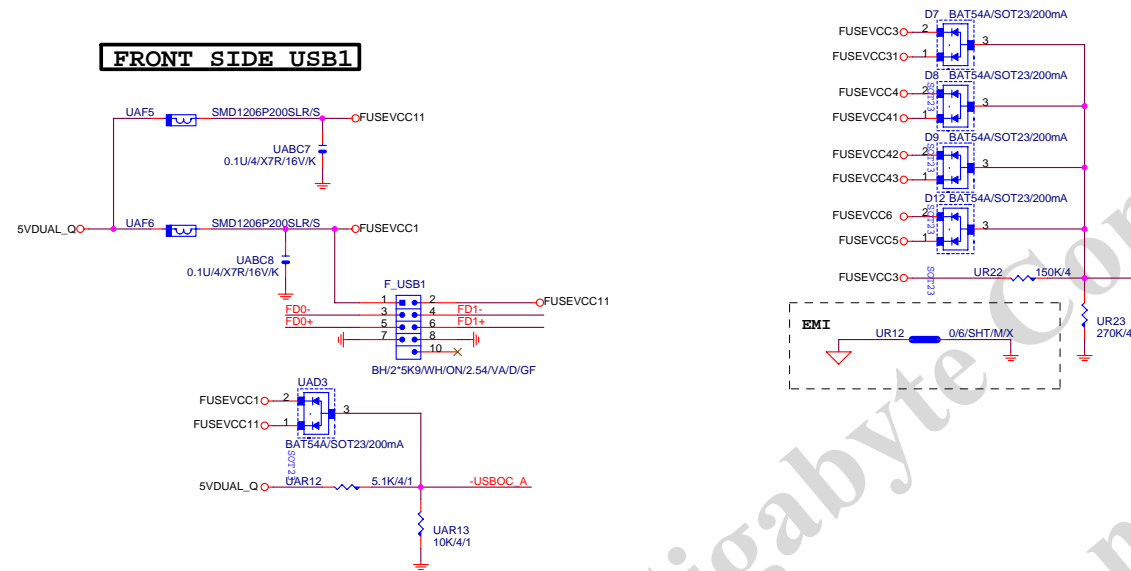


GIGABYTE

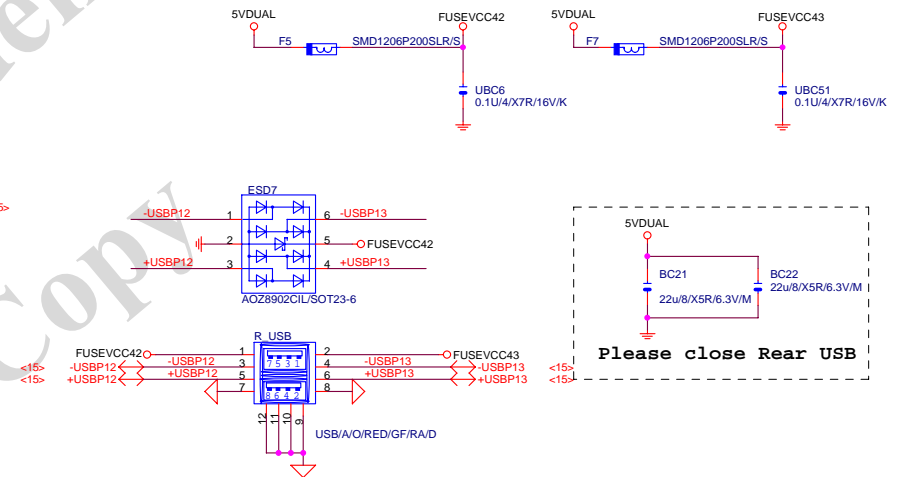
Title	ITE 8720 JX LPC IO ,Dual-BIOS ,TPM		
Size	Document Number	GA-990XA-UD3	Rev 1.11
Date:	Thursday, September 22, 2011	Sheet 21	of 35



FRONT SIDE USB1

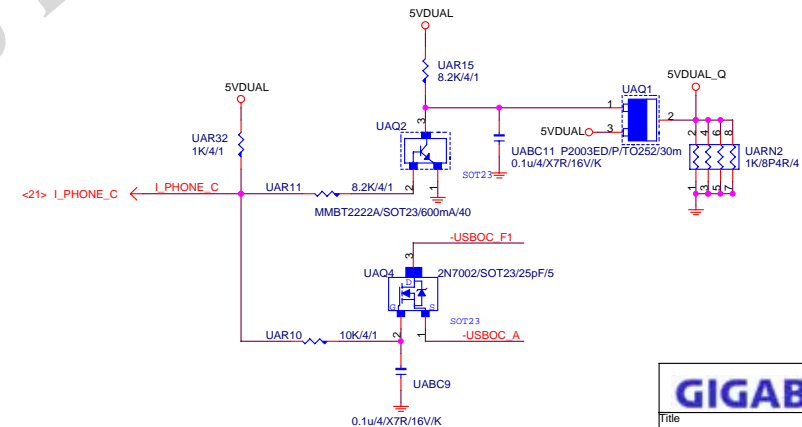
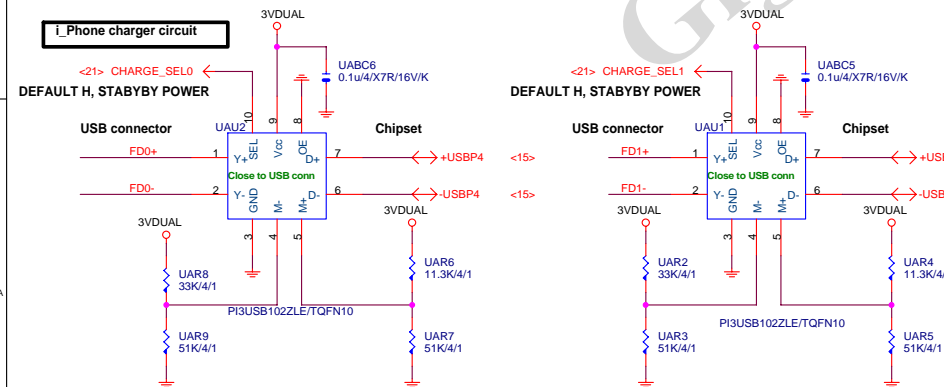


REAR USB



Please close Rear USB

I-Phone charger circuit

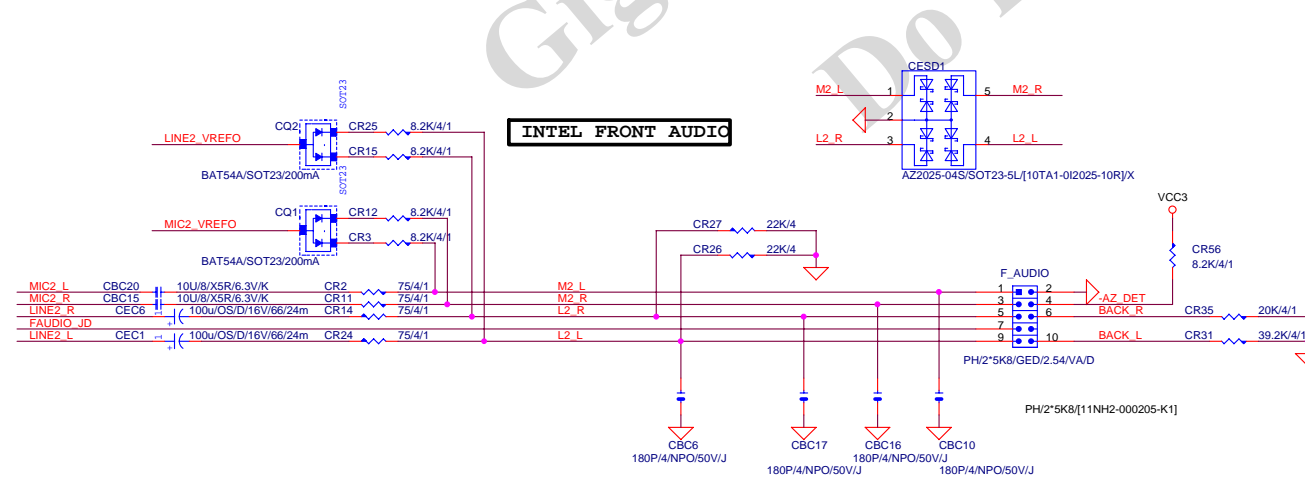
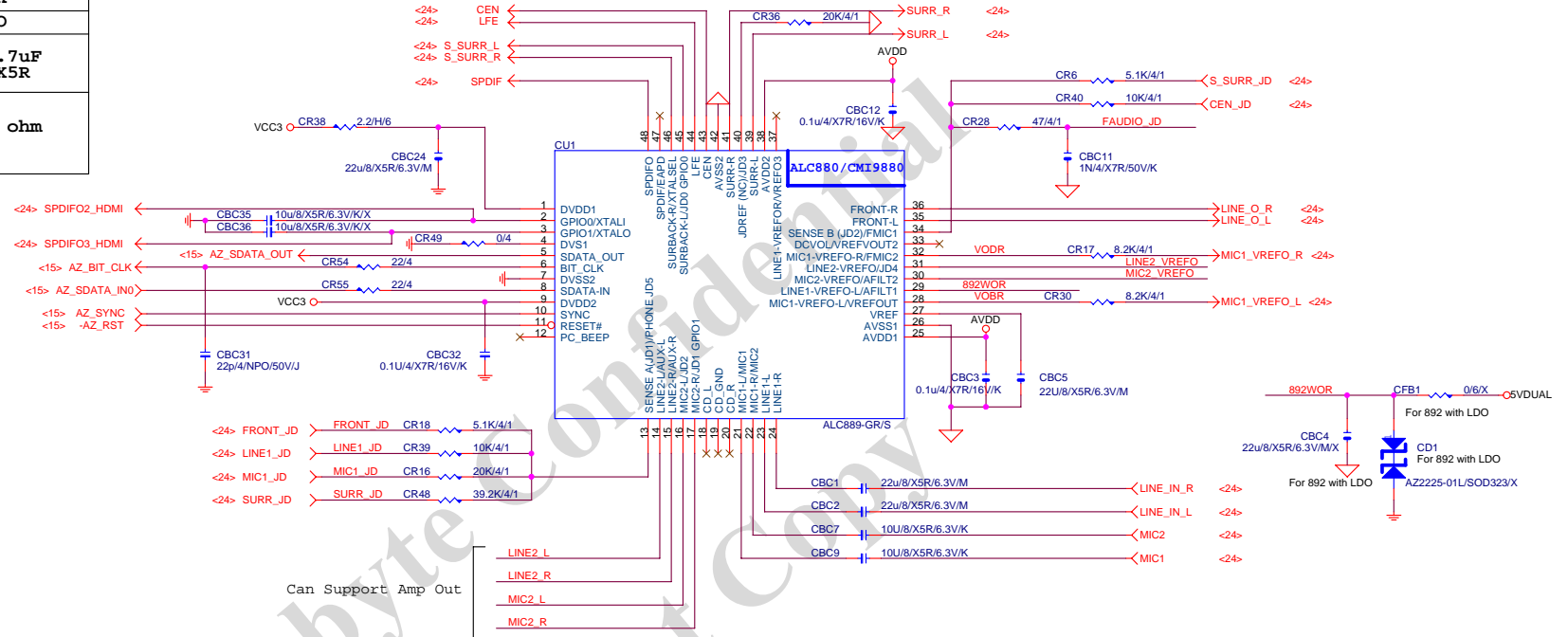


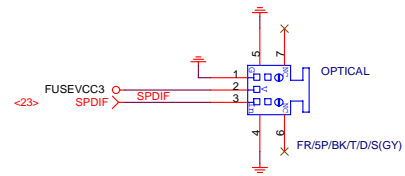
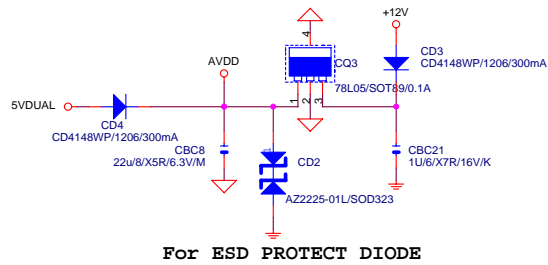
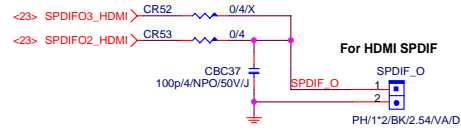
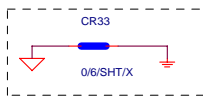
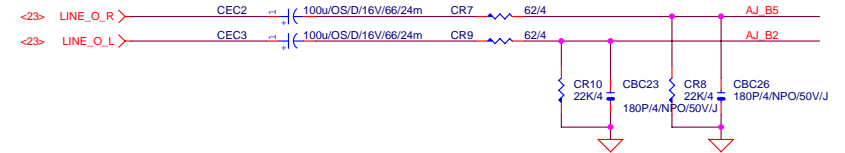
GIGABYTE®

COM/LPT/F_USB/PWR

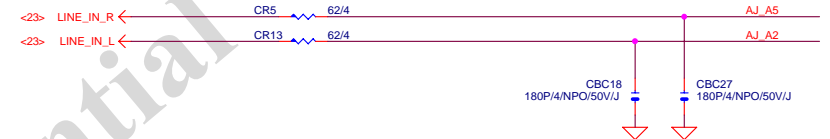
Title	COM/LPT/F_USB/PWR		Rev
Size	Document Number	GA-990XA-UD3	1.11
Date:	Wednesday, September 21, 2011	Sheet	22 of 35

	ALC892R	ALC889	ALC889A
CR16	X	X	O
CR24	X	X	O
CR25	X	O	O
CBC42	10uF/X5R	X	X
CR2	20K/1%	20K/1%	20K/0.1%
CR9	O	O	X
CR10	X	X	O
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R	10uF /X5R	4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR27/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm	66 ohm or lower	75 ohm

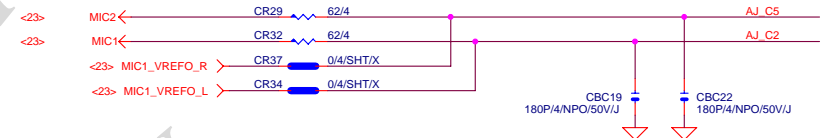


LINE OUT
FRONT OUT

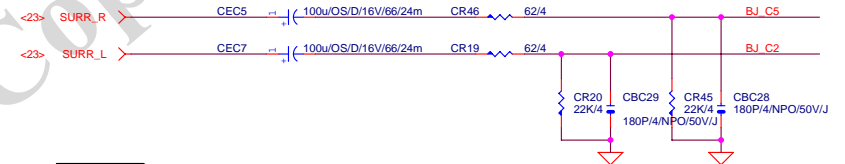
LINE-IN



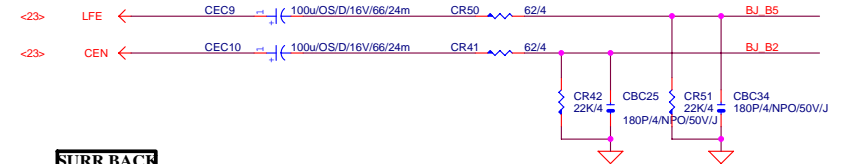
MIC



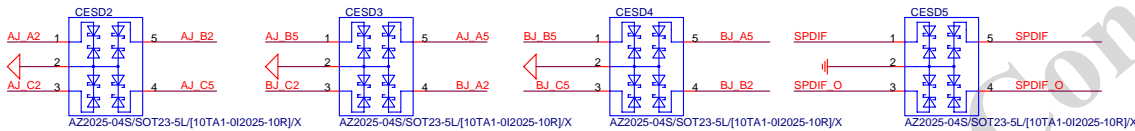
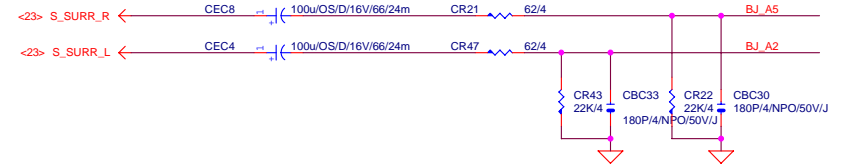
SURROUND



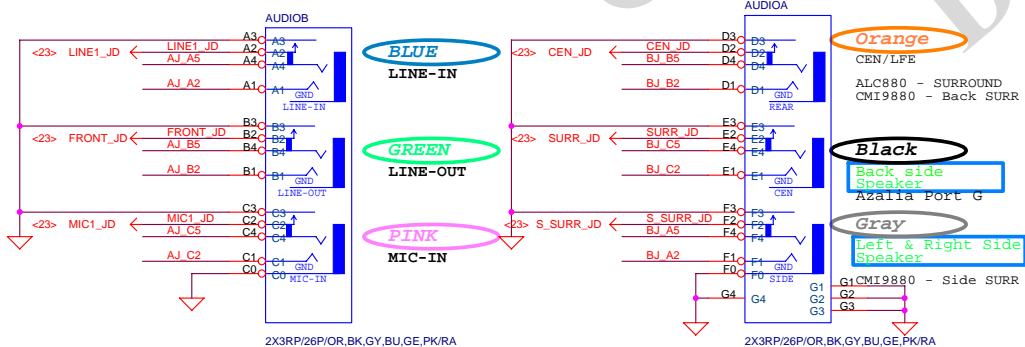
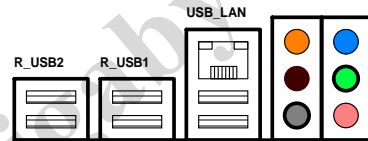
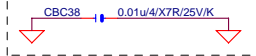
CEN/LFE



SURR BACK



For Audio precision test

A3R7/13P/B/[11NR6-403006-01_11NR6-403006-02]
3R3+15P/[11NR6-403004-11]A3R7/13P/B/[11NR6-403006-71]
3R3+15P/[11NR6-403004-31]

GIGABYTE

Title

AUDIO JACK

Size

Document Number

Cust

GA-990XA-UD3

Date

Wednesday, September 21, 2011

Sheet

24

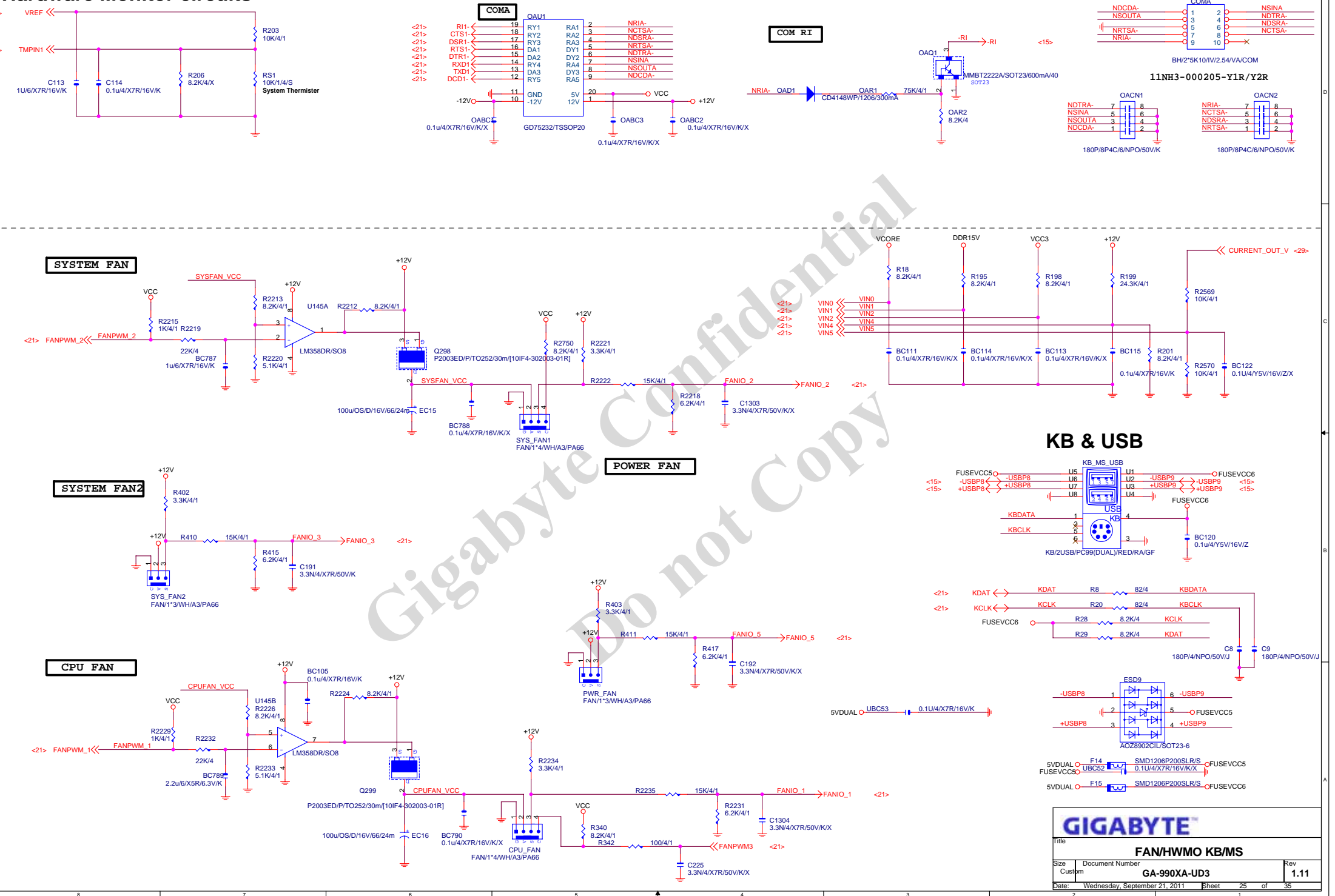
of

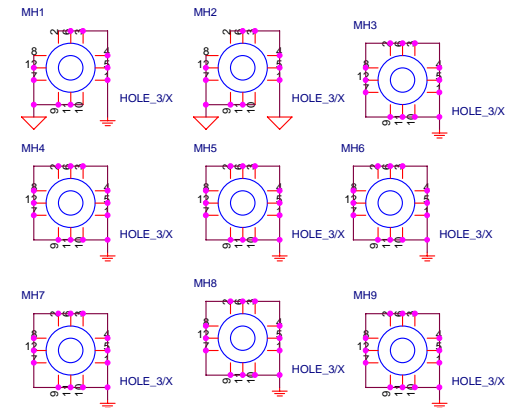
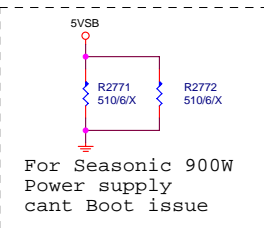
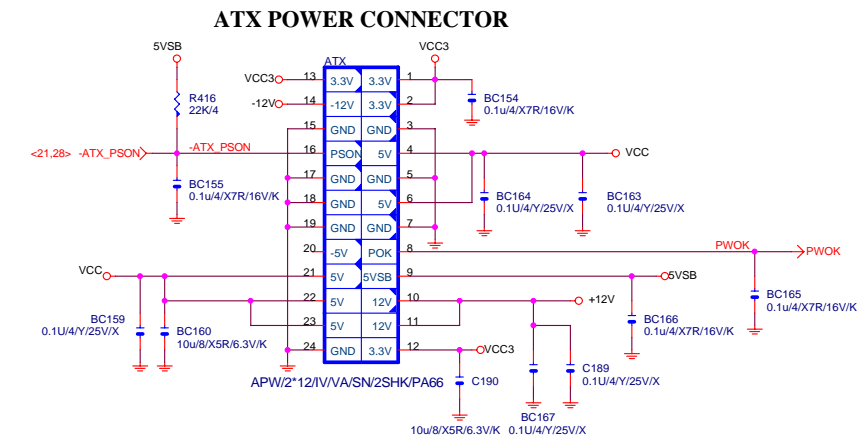
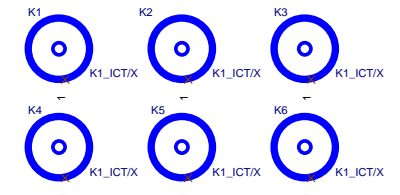
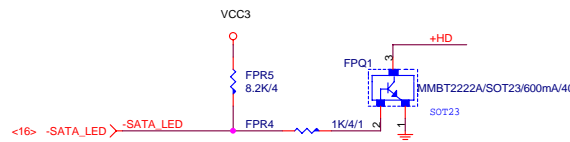
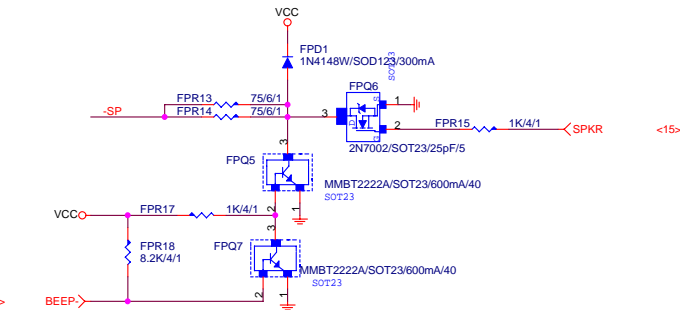
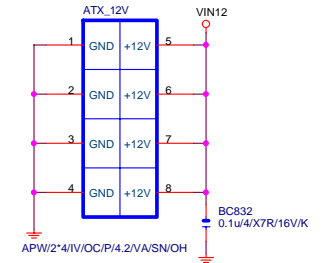
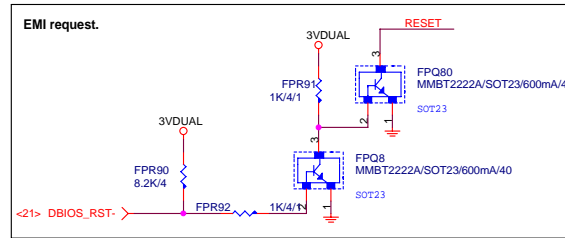
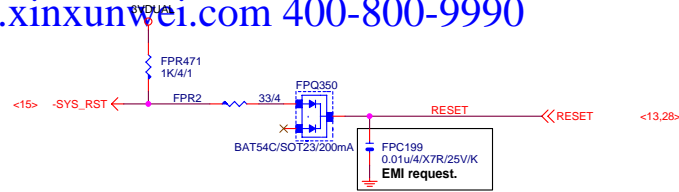
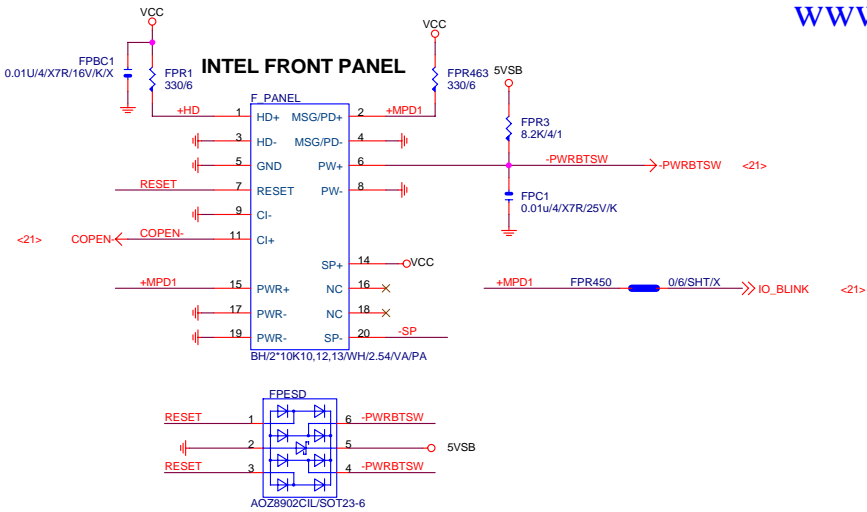
35

Rev

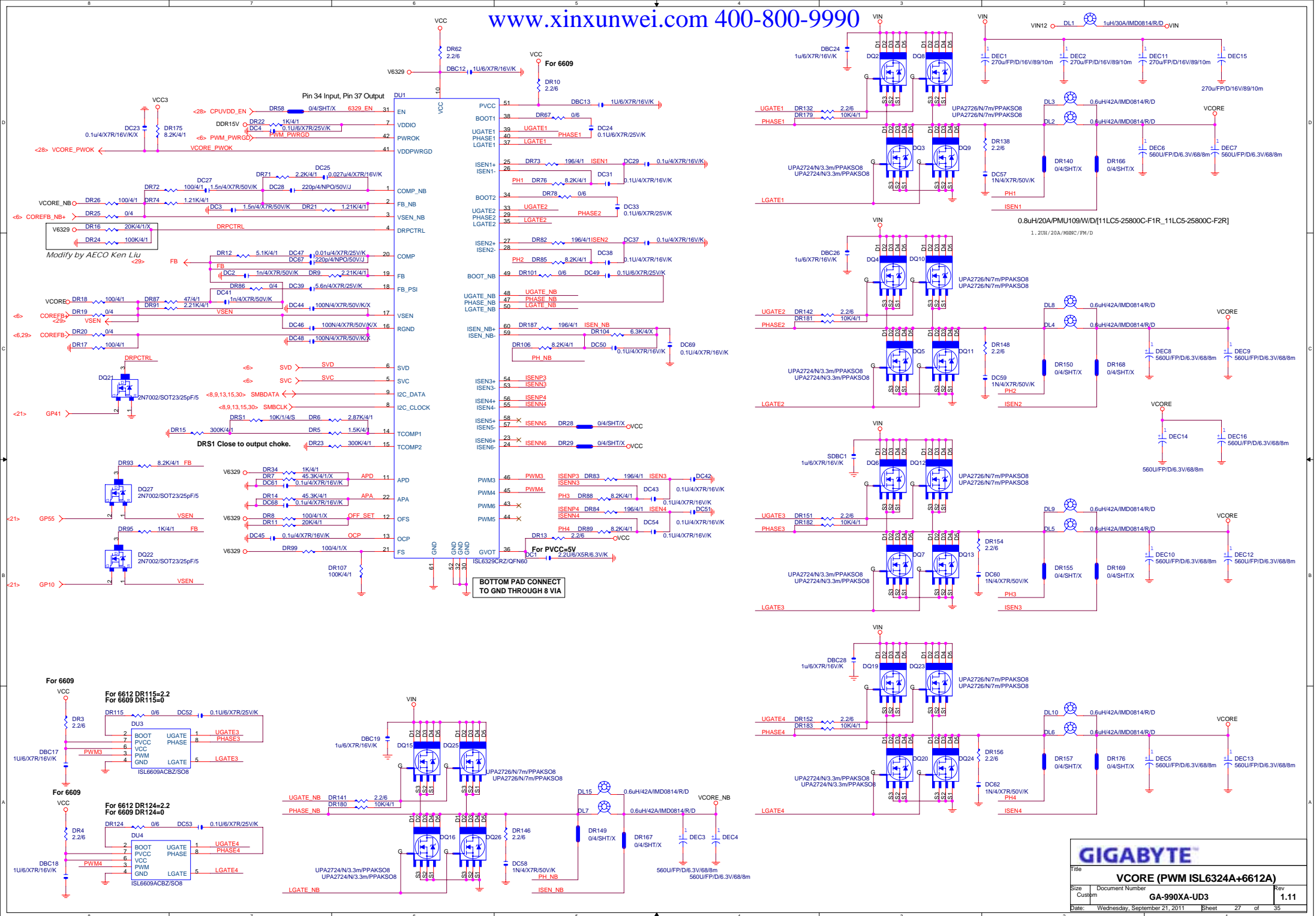
1.11

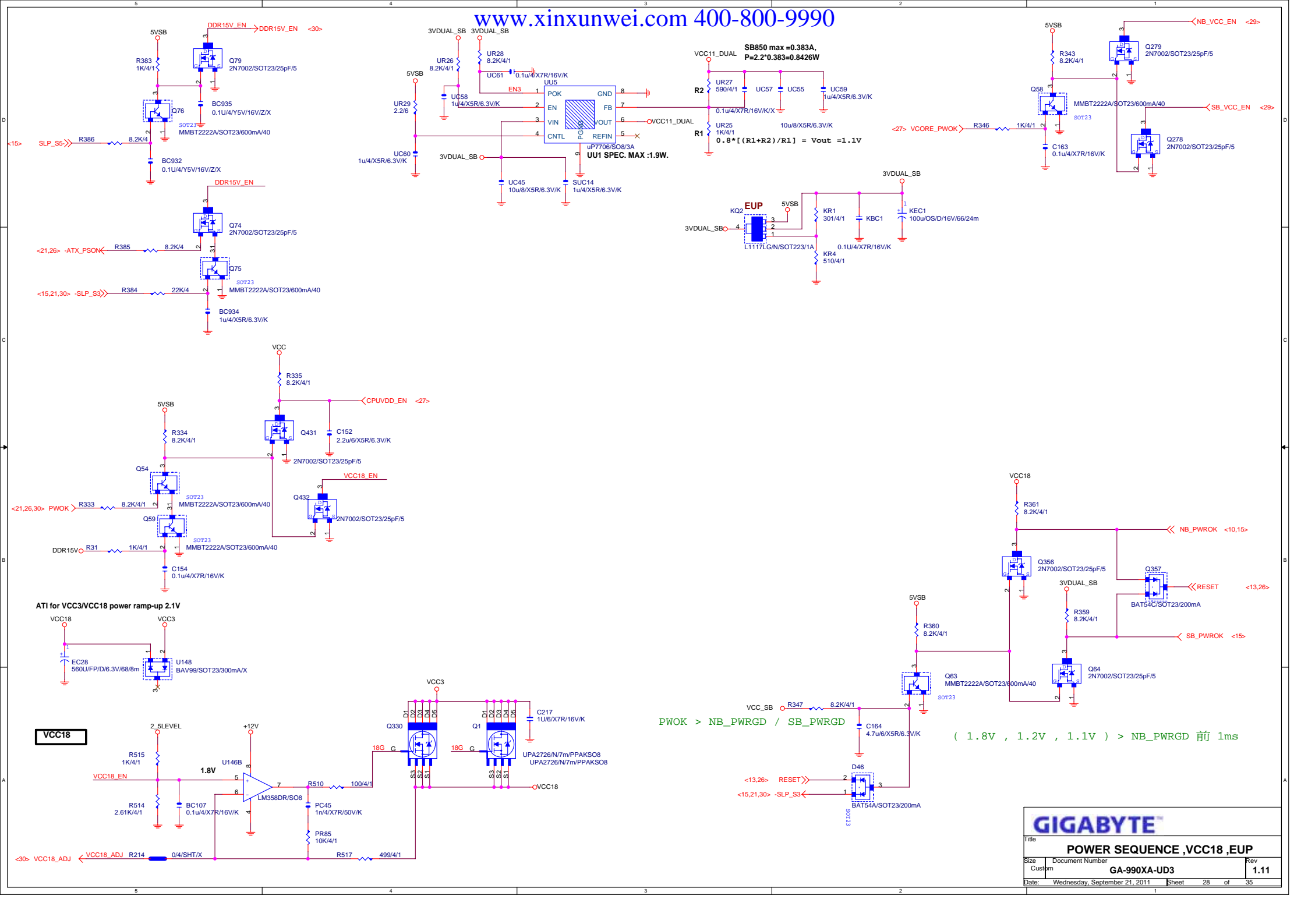
Hardware Monitor circuits





GIGABYTE			
Title			
ATX, FRONT PANEL ,EC			
Size	Document Number	Rev	
Custom	GA-990XA-UD3	1.11	
Date:	Wednesday, September 21, 2011	Sheet	26 of 35

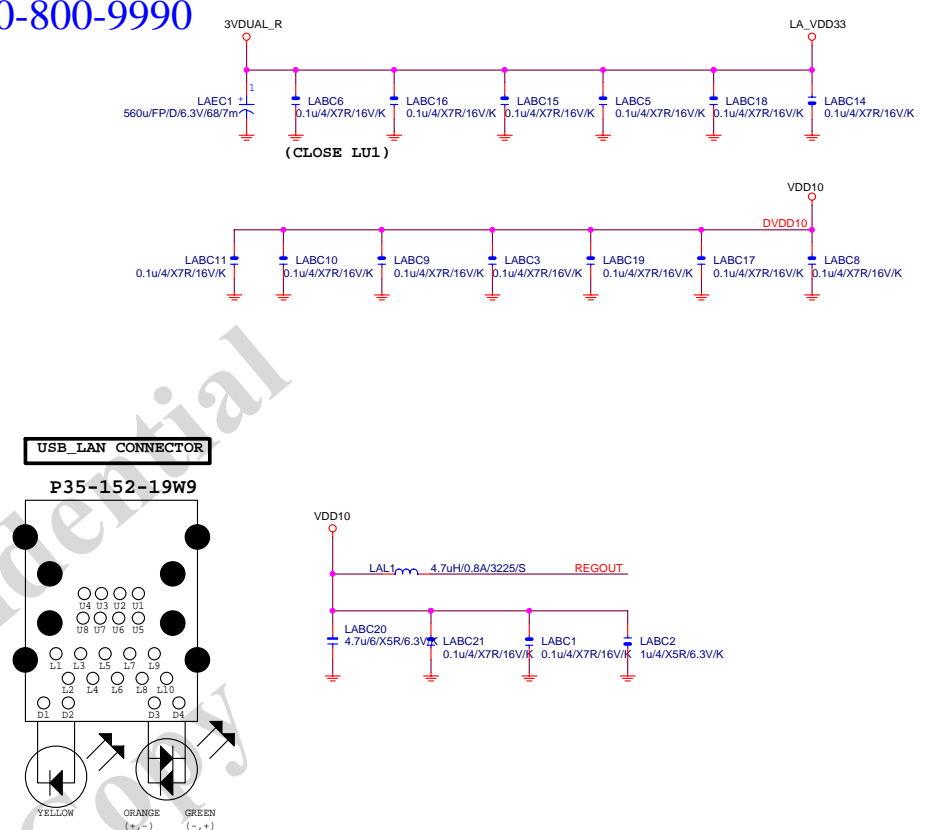
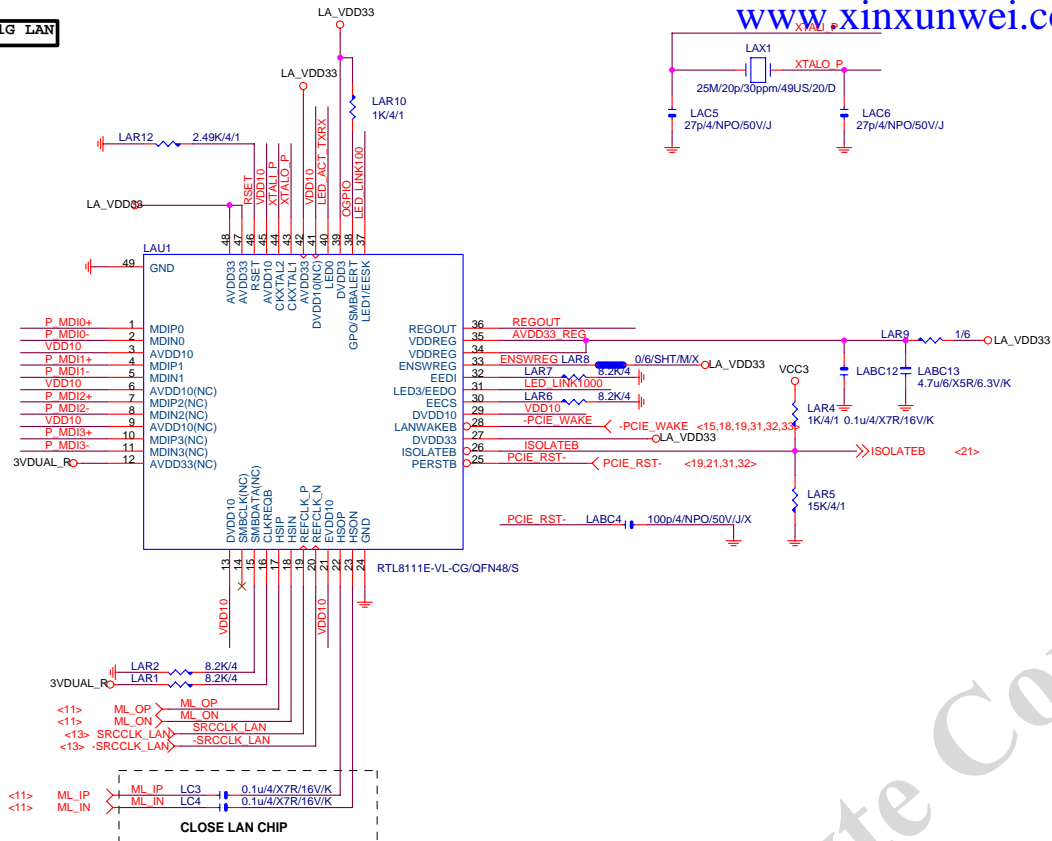




[illegible][illegible]

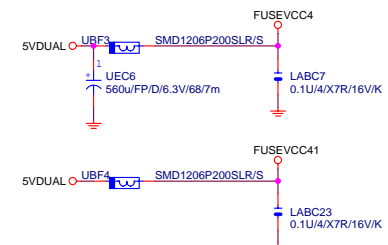
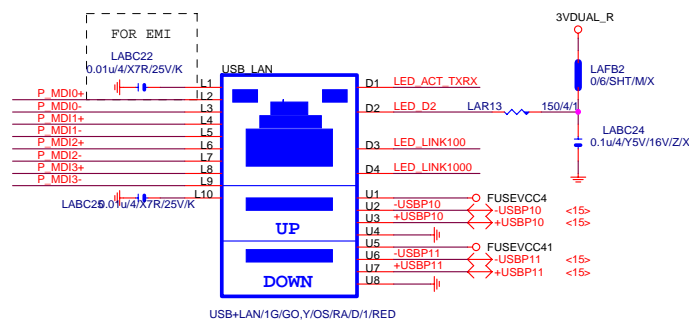


PCIE-1G LAN



USB_LAN

```
RTL8101E:LR38/LC5/LR43/LC6-->O
RTL8111C:LC6-->O
RTL8102E:LC5/LC6-->O
```



```

RTL8101E :L1+L10-->AVDD18+0.1U(BIOS  DISABLE MDI-X FUNCTION)
1G  :USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1

```

